

SEMICONDUCTOR DEVICES

Inventor: Michiru HOGYOKU

5 Applicant hereby incorporates by reference Japanese Application No. 2000-385530,
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Technical Field

10 The present invention relates to semiconductor devices and may include
semiconductor devices that are applied to a CMOS inverter circuit using a partially depleted
SOI – CMOSFET with a floating body.

Related Art

 A conventional semiconductor device is described below.

15 A CMOS inverter circuit using a partially depleted SOI (silicon on insulator) –
CMOSFET in certain forms may be considered as a conventional semiconductor device.
However, this CMOS inverter circuit in conventional form has a problem of duty cycle
dependency of input signals which results from substrate floating effects, which is observed
as an inverter delay time.

20 The following three semiconductor devices can be considered as means which may
solve the above described problem.

 As a first semiconductor device, a fully depleted SOI – MOSFET that does not show
the substrate floating effect may be used. Also, as a second semiconductor device, a
semiconductor device, in which a body is provided with a terminal and its potential is fixed
25 at a source potential to restrict the substrate floating effect, in other word, a body-tied-to-
source operation is conducted, may be used. Also, as a third semiconductor device, a
semiconductor device, in which a body is provided with a terminal and its potential is fixed
at a gate potential to restrict the substrate floating effect, in other word, a body-tied-to-gate
operation is conducted, may be used.

Brief Description of the Drawings

Embodiments of the invention are described with reference to the accompanying drawings which, for illustrative purposes, are schematic and not necessarily drawn to scale.

Fig. 1 shows a cross-sectional view of a semiconductor device in accordance with one embodiment of the present invention.

Fig. 2 shows a graph illustrating relations between the film thickness T_{SOI} of the SOI film and the amount of majority carriers in the body section in OUT-HIGH state and OUT-LOW state when the power supply voltage is set at 0.6 V and the impurity concentration of the body is changed.

Fig. 3 shows a graph illustrating relations between the film thickness T_{SOI} of the SOI film and the amount of majority carriers in the body section in OUT-HIGH state and OUT-LOW state when the power supply voltage is set at 0.8 V and the impurity concentration of the body is changed.

Fig. 4 shows a graph illustrating relations between the film thickness T_{SOI} of the SOI film and the amount of majority carriers in the body section in OUT-HIGH state and OUT-LOW state when the power supply voltage is set at 1.0 V and the impurity concentration of the body is changed.

Fig. 5 is a graph showing optimum values of the thickness of the SOI film with respect to a variety of impurity concentrations of the body and power supply voltages, which are obtained by conducting a linear interpolation of the results shown in Figs. 2 – 4.

Fig. 6 is a graph showing relations between the film thickness of the SOI film and transient threshold voltages. Reference number 51 indicates the case in OUT-HIGH state, and reference number 52 indicates the case in OUT-LOW state.

Fig. 7 is a graph showing relations between the impurity concentration of the body and transient threshold voltages. Reference number 53 indicates the case in OUT-HIGH state, and reference number 54 indicates the case in OUT-LOW state.

Detailed Description

Problems with the three semiconductor devices described above in the related art section include the following. When the first semiconductor device is used, the SOI layer needs to be made extremely thin in order to restrict the short-channel effect (resulting in a lowered threshold voltage and an increased sub-threshold coefficient). It is very difficult to control the reduction of the film thickness of such a SOI layer, the controllability in the electric characteristics deteriorates in association with such an extreme reduction of the film thickness of the SOI layer, and the contact resistance of the source/drain regions increases. Therefore, the use of the first semiconductor device is not generally desired.

Also, when the second semiconductor device is used, a terminal needs to be provided on the body, which results in a problem in that the area per element increases. Therefore, the use of the second semiconductor device is also not generally desired.

Further, when the third semiconductor device is used, not only does the area per element increase, but also the gate capacity increases. Therefore, the use of the third semiconductor device is also not generally desired.

In view of all the above, a partially depleted SOI – CMOSFET with a floating body may be used to seek a solution to solve the problem of duty cycle dependency of input signals which results from substrate floating effects, which is observed as an inverter delay time.

Preferred embodiments of the present invention has been made in view of the circumstances described above. It is an object of certain embodiments to provide a semiconductor device that solves the problem of the duty cycle dependency.

To solve the problems described above, embodiments of the present invention relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.6 V is used, a thickness of the SOI film is 0.084 μm or greater and 0.094

μm or smaller, and an impurity concentration of the SOI film is $7.95 \times 10^{17}/\text{cm}^3$ or greater and $8.05 \times 10^{17}/\text{cm}^3$ or smaller.

By the semiconductor device described above, the film thickness of the SOI film, the impurity concentration of the SOI film, and the power supply voltage are adjusted such that the total amounts of the body majority carriers under steady state in both of the bias conditions in an OUT-HIGH (IN-LOW) state and an OUT-LOW (IN-HIGH) state become generally equal to each other. By this control, the problem of duty cycle dependency of input signals, which is observed as an inverter delay time is solved. This is discussed in detail in a document entitled "Minimizing Floating Body-Induced Threshold Voltage Variation in Partially Depleted SOI CMOS" in IEEE Electron Device Lett., vol. 17, p. 391, Aug. 1996, by A Wei et al.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.6 V is used, a thickness of the SOI film is 0.089 μm or greater and 0.099 μm or smaller, and an impurity concentration of the SOI film is $8.95 \times 10^{17}/\text{cm}^3$ or greater and $9.05 \times 10^{17}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.6 V is used, a thickness of the SOI film is 0.093 μm or greater and 0.103 μm or smaller, and an impurity concentration of the SOI film is $0.095 \times 10^{18}/\text{cm}^3$ or greater and $1.005 \times 10^{18}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor

substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.6 V is used, a thickness of the SOI film is 0.096 μm or greater and 0.106 μm or smaller, and an impurity concentration of the SOI film is $1.095 \times 10^{18}/\text{cm}^3$ or greater and $1.105 \times 10^{18}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.6 V is used, a thickness of the SOI film is 0.100 μm or greater and 0.110 μm or smaller, and an impurity concentration of the SOI film is $1.195 \times 10^{18}/\text{cm}^3$ or greater and $1.205 \times 10^{18}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.8 V is used, a thickness of the SOI film is 0.068 μm or greater and 0.078 μm or smaller, and an impurity concentration of the SOI film is $7.95 \times 10^{17}/\text{cm}^3$ or greater and $8.05 \times 10^{17}/\text{cm}^3$ or smaller.

A semiconductor device in accordance with the present invention pertains to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.8 V is used, a thickness of the SOI film is 0.074 μm or greater and 0.084

μm or smaller, and an impurity concentration of the SOI film is $8.95 \times 10^{17}/\text{cm}^3$ or greater and $9.05 \times 10^{17}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.8 V is used, a thickness of the SOI film is 0.078 μm or greater and 0.088 μm or smaller, and an impurity concentration of the SOI film is $0.095 \times 10^{18}/\text{cm}^3$ or greater and $1.005 \times 10^{18}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.8 V is used, a thickness of the SOI film is 0.083 μm or greater and 0.093 μm or smaller, and an impurity concentration of the SOI film is $1.095 \times 10^{18}/\text{cm}^3$ or greater and $1.105 \times 10^{18}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.8 V is used, a thickness of the SOI film is 0.087 μm or greater and 0.097 μm or smaller, and an impurity concentration of the SOI film is $1.195 \times 10^{18}/\text{cm}^3$ or greater and $1.205 \times 10^{18}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a

gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 1.0 V is used, a thickness of the SOI film is 0.057 μm or greater and 0.067 μm or smaller, and an impurity concentration of the SOI film is $7.95 \times 10^{17}/\text{cm}^3$ or greater and $8.05 \times 10^{17}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 1.0 V is used, a thickness of the SOI film is 0.063 μm or greater and 0.073 μm or smaller, and an impurity concentration of the SOI film is $8.95 \times 10^{17}/\text{cm}^3$ or greater and $9.05 \times 10^{17}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 1.0 V is used, a thickness of the SOI film is 0.068 μm or greater and 0.078 μm or smaller, and an impurity concentration of the SOI film is $0.095 \times 10^{18}/\text{cm}^3$ or greater and $1.005 \times 10^{18}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 1.0 V is used, a thickness of the SOI film is 0.072 μm or greater and 0.082 μm or smaller, and an impurity concentration of the SOI film is $1.095 \times 10^{18}/\text{cm}^3$ or greater and $1.105 \times 10^{18}/\text{cm}^3$ or smaller.

Embodiments also relate to a semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising: a dielectric film formed on a semiconductor substrate; a SOI film composed of single crystal Si formed on the dielectric layer film; a gate dielectric film formed on the SOI film; a gate electrode formed on the gate dielectric film; and a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 1.0 V is used, a thickness of the SOI film is 0.076 μm or greater and 0.086 μm or smaller, and an impurity concentration of the SOI film is $1.195 \times 10^{18}/\text{cm}^3$ or greater and $1.205 \times 10^{18}/\text{cm}^3$ or smaller.

Certain preferred embodiments of the present invention are described below with reference to the accompanying drawings.

Fig. 1 shows a cross-sectional view of a semiconductor device in accordance with one embodiment of the present invention. The semiconductor device is a partially depleted SOI – CMOSFET that is used for a CMOS inverter circuit.

The semiconductor device has a silicon substrate 1, and a BOX layer (dielectric film) 2 formed on the silicon substrate 1. A SOI film (body) 3 that is preferably composed of single crystal Si having a thickness of T_{SOI} is formed on the BOX layer 2. A gate oxide layer 4 is formed on the SOI film 3, and a gate electrode 5 is formed on the gate oxide layer 4. In the SOI film 3, a low concentration impurity diffusion layer 6 is formed in a LDD (lightly doped drain) region, and diffusion layers 7 and 8 for source/drain regions are formed in source/drain regions. Also, a back gate electrode 9 is formed below the silicon substrate 1.

By using the partially depleted SOI – CMOSFET described above, a method is adopted to solve the problem of duty cycle dependency of input signals which results from the substrate floating effect, which is observed as an inverter delay time. According to the method, the film thickness of the SOI film, the impurity concentration distribution of the SOI film (body), and the power supply voltage V_{dd} are adjusted such that the total amounts of the body majority carriers under steady state in both of the bias conditions in an OUT-HIGH (IN-LOW) state and an OUT-LOW (IN-HIGH) state become generally equal to each other. By this control, the problem of duty cycle dependency of input signals, which is

observed as an inverter delay time, is solved. This is discussed in detail in a document entitled “Minimizing Floating Body-Induced Threshold Voltage Variation in Partially Depleted SOI CMOS” in IEEE Electron Device Lett., vol. 17, p. 391, Aug. 1996, by A Wei et al.

5 Next, specific examples of how the film thickness of the SOI film, the impurity concentration distribution of the SOI film (body), and the power supply voltage V_{dd} are adjusted are described.

Simulations to optimize the thickness of a SOI film can be performed by a two-dimensional device analysis in connection with the duty cycle dependency of input signals, 10 which is observed as an inverter delay time.

Structural parameters of partially depleted SOI – MOSFETs that re used in the two-dimensional analysis are as follows.

Gate length: 0.18 μm

Gate sidewall width: 0.07 μm

15 Impurity diffusion length of source/drain/LDD: 0.04 μm

Thickness T_{SOI} of SOI: 0.06 μm, 0.065 μm, 0.07 μm, 0.075 μm, 0.08 μm, 0.085 μm, 0.09 μm, 0.095 μm, 0.1 μm, 0.105 μm, 0.11 μm, 0.115 μm, or 0.12 μm

Thickness of gate oxide film: 0.004 μm

Thickness of BOX layer (Embedded oxide film): 0.4 μm

20 Thickness of silicon substrate: 0.4 μm

Junction depth T_{LDD} of LDD: 0.07 μm

Impurity concentration of the body (assuming it spatially uniformly distributes): $8 \times 10^{17}/\text{cm}^3$, $9 \times 10^{17}/\text{cm}^3$, $1 \times 10^{18}/\text{cm}^3$, $1.1 \times 10^{18}/\text{cm}^3$, $1.2 \times 10^{18}/\text{cm}^3$

Maximum value of impurity concentration of source/drain regions: $5 \times 10^{20}/\text{cm}^3$

25 Maximum value of impurity concentration of LDD: $1 \times 10^{19}/\text{cm}^3$

Impurity concentration of silicon substrate: $5 \times 10^{14}/\text{cm}^3$

Three power supply voltages V_{dd} at 0.6 V, 0.8 V and 1.0 V are assumed. The work function of the gate electrode is 4.17 V, assuming the case of n⁺ polysilicon.

The analysis is performed by relying on a drift – diffusion model which is represented by a sum of a drift term that proportions the flow of carriers to an electric field and a diffusion term that proportions the same to a concentration gradient. Both carriers of electrons and holes are expressly treated, and SRH (Shockley Read Hall) recombination that is dependent on the impurity concentration and band-gap narrowing effects are considered, along with Auger recombination. As a parameter for SRH recombination, a default value: $\tau_n = \tau_p = 0.1 \mu\text{sec}$ is used. The concentration of carriers is evaluated by Boltzmann statistic. It is assumed that the entire impurity is ionized. It is noted that the impact ionization and inter-band tunneling are not considered as low power supply voltages are assumed. Also, the carrier energy balance equation or the lattice thermal flow equation is not considered.

Next, results of the two-dimensional device analysis are described.

The total amounts of body majority carriers in both OUT-HIGH and OUT-LOW device conditions under steady state are calculated. It is noted that the device analysis is conducted in two-dimensional, such that the total amount of body majority carriers is standardized with the channel width: w (the unit is $1/\text{m}$).

Fig. 2 shows a graph illustrating relations between the film thickness T_{SOI} of the SOI film and the amount of majority carriers in the body section in the OUT-HIGH state and the OUT-LOW state when the power supply voltage is set at 0.6 V and the impurity concentration of the body is changed.

Reference number 11 pertains to the OUT-HIGH state with the impurity concentration of the body being $8 \times 10^{17}/\text{cm}^3$. Reference number 12 pertains to the OUT-LOW state with the impurity concentration of the body being $8 \times 10^{17}/\text{cm}^3$. Reference number 13 pertains to the OUT-HIGH state with the impurity concentration of the body being $9 \times 10^{17}/\text{cm}^3$. Reference number 14 pertains to the OUT-LOW state with the impurity concentration of the body being $9 \times 10^{17}/\text{cm}^3$. Reference number 15 pertains to the OUT-HIGH state with the impurity concentration of the body being $1 \times 10^{18}/\text{cm}^3$. Reference number 16 pertains to the OUT-LOW state with the impurity concentration of the body being $1 \times 10^{18}/\text{cm}^3$. Reference number 17 pertains to the OUT-HIGH state with the impurity concentration of the body being $1.1 \times 10^{18}/\text{cm}^3$. Reference number 18 pertains to

the OUT-LOW state with the impurity concentration of the body being $1.1 \times 10^{18}/\text{cm}^3$.

Reference number 19 pertains to the OUT-HIGH state with the impurity concentration of the body being $1.2 \times 10^{18}/\text{cm}^3$. Reference number 20 pertains to the OUT-LOW state with the impurity concentration of the body being $1.2 \times 10^{18}/\text{cm}^3$.

5 Fig. 3 shows a graph illustrating relations between the film thickness T_{SOI} of the SOI film and the amount of majority carriers in the body section in the OUT-HIGH state and the OUT-LOW state when the power supply voltage is set at 0.8 V and the impurity concentration of the body is changed.

Reference number 21 pertains to the OUT-HIGH state with the impurity
10 concentration of the body being $8 \times 10^{17}/\text{cm}^3$. Reference number 22 pertains to the OUT-LOW state with the impurity concentration of the body being $8 \times 10^{17}/\text{cm}^3$. Reference number 23 pertains to the OUT-HIGH state with the impurity concentration of the body being $9 \times 10^{17}/\text{cm}^3$. Reference number 24 pertains to the OUT-LOW state with the impurity concentration of the body being $9 \times 10^{17}/\text{cm}^3$. Reference number 25 pertains to
15 the OUT-HIGH state with the impurity concentration of the body being $1 \times 10^{18}/\text{cm}^3$. Reference number 26 pertains to the OUT-LOW state with the impurity concentration of the body being $1 \times 10^{18}/\text{cm}^3$. Reference number 27 pertains to the OUT-HIGH state with the impurity concentration of the body being $1.1 \times 10^{18}/\text{cm}^3$. Reference number 28 pertains to the OUT-LOW state with the impurity concentration of the body being $1.1 \times 10^{18}/\text{cm}^3$.
20 Reference number 29 pertains to the OUT-HIGH state with the impurity concentration of the body being $1.2 \times 10^{18}/\text{cm}^3$. Reference number 30 pertains to the OUT-LOW state with the impurity concentration of the body being $1.2 \times 10^{18}/\text{cm}^3$.

Fig. 4 shows a graph illustrating relations between the film thickness T_{SOI} of the SOI film and the amount of majority carriers in the body section in the OUT-HIGH state and the
25 OUT-LOW state when the power supply voltage is set at 1.0 V and the impurity concentration of the body is changed.

Reference number 31 pertains to the OUT-HIGH state with the impurity concentration of the body being $8 \times 10^{17}/\text{cm}^3$. Reference number 32 pertains to the OUT-

LOW state with the impurity concentration of the body being $8 \times 10^{17}/\text{cm}^3$. Reference number 33 pertains to the OUT-HIGH state with the impurity concentration of the body being $9 \times 10^{17}/\text{cm}^3$. Reference number 34 pertains to the OUT-LOW state with the impurity concentration of the body being $9 \times 10^{17}/\text{cm}^3$. Reference number 35 pertains to the OUT-HIGH state with the impurity concentration of the body being $1 \times 10^{18}/\text{cm}^3$. Reference number 36 pertains to the OUT-LOW state with the impurity concentration of the body being $1 \times 10^{18}/\text{cm}^3$. Reference number 37 pertains to the OUT-HIGH state with the impurity concentration of the body being $1.1 \times 10^{18}/\text{cm}^3$. Reference number 38 pertains to the OUT-LOW state with the impurity concentration of the body being $1.1 \times 10^{18}/\text{cm}^3$. Reference number 39 pertains to the OUT-HIGH state with the impurity concentration of the body being $1.2 \times 10^{18}/\text{cm}^3$. Reference number 40 pertains to the OUT-LOW state with the impurity concentration of the body being $1.2 \times 10^{18}/\text{cm}^3$.

Referring to Figs. 2 – 4, a point at which curves in the OUT-HIGH state and the OUT-LOW state at the same impurity concentration in the body section overlap one another is where the amounts of majority carriers become equal to one another, and represents an optimum film thickness of the SOI film that can avoid the problem of duty cycle dependency of input signals which is observed as an inverter delay time. Relations between the film thickness and impurity concentrations are shown in Fig. 5.

Fig. 5 is a graph showing optimum values of the thickness of the SOI film with respect to a variety of impurity concentrations of the body and power supply voltages, which are obtained by conducting a linear interpolation of the results shown in Figs. 2 – 4.

Reference number 41 indicates the relation between impurity concentrations of the body and optimum film thickness of the SOI film when the power supply voltage is 1.0 V. Reference number 42 indicates the relation between impurity concentrations of the body and optimum film thickness of the SOI film when the power supply voltage is 0.8 V. Reference number 43 indicates the relation between impurity concentrations of the body and optimum film thickness of the SOI film when the power supply voltage is 0.6 V.

Next, transient transfer characteristics with the steady states under OUT-HIGH and OUT-LOW bias conditions as being initial device internal states are analyzed, to thereby

calculate transient threshold voltages. It is noted that an example in which the power supply voltage is 0.8 V is employed.

Fig. 6 is a graph showing relations between the film thickness of the SOI film and transient threshold voltages when the impurity concentration of the body is $1 \times 10^{18}/\text{cm}^{-3}$.

5 Reference number 51 indicates the case in OUT-HIGH state, and reference number 52 indicates the case in OUT-LOW state.

According to the graph, a point where both of the lines cross one another is where the threshold values as being the electrical characteristics concur with one another, and this point indicates an optimum value. Also, in one embodiment, when a margin of $\pm 0.5\%$ is
10 given for the transient threshold voltage at the optimum thickness of the SOI film, it is understood that variations in the thickness of the SOI film of about $\pm 0.005 \mu\text{m}$ may be permitted.

Also, Fig. 7 is a graph showing relations between the impurity concentration of the body and transient threshold voltages when the film thickness of the SOI film is $0.08 \mu\text{m}$.

15 Reference number 53 indicates the case in OUT-HIGH state, and reference number 54 indicates the case in OUT-LOW state.

According to the graph, a point where both of the lines cross one another is where the threshold values as being the electrical characteristics concur with one another, and this point indicates an optimum value. Also, in one embodiment, when a margin of $\pm 0.5\%$ is
20 given for the transient threshold voltage at the optimum impurity concentration of the body, it is understood that variations in the impurity concentration of the body of about $\pm 0.05 \times 10^{17} (= \pm 0.005 \times 10^{18})/\text{cm}^3$ may be permitted.

In view of the above, in the semiconductor device shown in Fig. 1, the optimum thickness of the SOI film, the impurity concentration of the body (SOI film) and the power
25 supply voltage Vdd which can solve the problem of duty cycle dependency of input signals, which is observed as an inverter delay time, are as follows.

When a power supply voltage of 0.6 V is used, the SOI film may preferably have a thickness of $0.089 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(8 \pm 0.05) \times 10^{17}/\text{cm}^3$. Also, the SOI film may preferably have a thickness

of $0.094 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(9 \pm 0.05) \times 10^{17}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.098 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1 \pm 0.005) \times 10^{18}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.101 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1.1 \pm 0.005) \times 10^{18}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.105 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1.2 \pm 0.005) \times 10^{18}/\text{cm}^3$.

When a power supply voltage of 0.8 V is used, the SOI film may preferably have a thickness of $0.073 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(8 \pm 0.05) \times 10^{17}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.079 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(9 \pm 0.05) \times 10^{17}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.083 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1 \pm 0.005) \times 10^{18}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.088 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1.1 \pm 0.005) \times 10^{18}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.092 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1.2 \pm 0.005) \times 10^{18}/\text{cm}^3$.

When a power supply voltage of 1.0 V is used, the SOI film may preferably have a thickness of $0.062 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(8 \pm 0.05) \times 10^{17}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.068 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(9 \pm 0.05) \times 10^{17}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.073 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1 \pm 0.005) \times 10^{18}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.077 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1.1 \pm 0.005) \times 10^{18}/\text{cm}^3$. Also, the SOI film may preferably have a thickness of $0.081 \pm 0.005 \mu\text{m}$, and the SOI film may preferably have an impurity concentration of $(1.2 \pm 0.005) \times 10^{18}/\text{cm}^3$.

In accordance with the embodiments described above, technical resources for controlling the short-channel effect more than those required for bulk CMOSFETs are not required, a controllability of the electric characteristic can be obtained at a similar level obtained by bulk CMOSFETs, the area per element and the gate capacity do not increase,
5 and the problem of duty cycle dependency of input signals which characteristically occurs in body floating controlled partially depleted SOI – CMOSFETs can be avoided.

It is noted that the present invention is not limited to the embodiments described above, and many modifications can be made.

As described above, in accordance with certain embodiments of the present
10 invention, the film thickness of a SOI film, the impurity concentration of the SOI film, and the power supply voltage are adjusted such that the total amounts of the body majority carriers under steady state in both of the bias conditions in an OUT-HIGH (IN-LOW) state and an OUT-LOW (IN-HIGH) state become generally equal to each other. By this control,
15 the problem of duty cycle dependency of input signals, which is observed as an inverter delay time, may be solved.